Design Of DSBSC Modulator Using MOS Transistor And Analysis Of Its Power, Delay, Frequency Response And Thermal Noise Due To Channel Resistance Of MOS

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Abstract— This paper presents the design of double side band suppressed carrier (DSBSC) modulator using MOS transistors at deep sub micron level. Modulator part of the circuit has been designed using two transistor only. Working principle of the circuit has been presented qualitatively. Graphical representation of instantaneous power drawn from message signal source has been focused . Power consumption across the resistances in the inverting amplifier section has been measured. It is also measured the delay from carrier input instance to modulated output instance . Frequency response of the circuit has been plotted . Finally it is analysed the thermal noise of the circuit at output due to channel resistance of MOS transistor .All the measurements and analysis are performed using Tanner SPICE (T-SPICE) software . It is found that power drawn from the message signal source is of the order of 10^{-5} Watt . Said delay is of the order of pico second . The circuit exhibits very wide frequency range of operation without attenuation and higher cut off frequency is around 188GHz. From noise analysis it is found that thermal noise at output due to channel resistance is of the order of 10^{-24} $Volt^2$ /Hz.

Index Terms — DSBSC,modulation,delay,power ,thermal noise,frequency response ,T-SPICE,Schematic

1. INTRODUCTION

Modulation is a process by which some characteristics of a signal known as carrier signal is varied according to the base band signal or modulating signal or message signal . In this paper DSBSC modulator is designed using MOS transistor with feature size of 150nm. The circuit is designed to operate with square wave as carrier input. Carrier source is basically a clock pulse generator . CMOS inverter is designed to invert clock pulse to be used in the circuit . One buffer amplifier is designed with one voltage controlled voltage source having 2 MΩ input resistance and 75 Ω output resistance and open loop gain of 2×10^5 .With same input and output resistance another voltage controlled voltage source is used to realize inverting amplifier having overall gain equals to -1 .Inverting amplifier is used only to change the phase of the modulating signal by 180^0 . Buffer amplifier is used to avoid loading effect . Power, delay, thermal noise for specific part of the circuit are analyzed. Frequency of response of the circuit is also plotted.

II. SCHEMATIC DIAGRAM AND OPERATION OF THE CIRCUIT

A. Circuit description

The schematic diagram of proposed DSBSC modulator circuit is shown in figure1 .

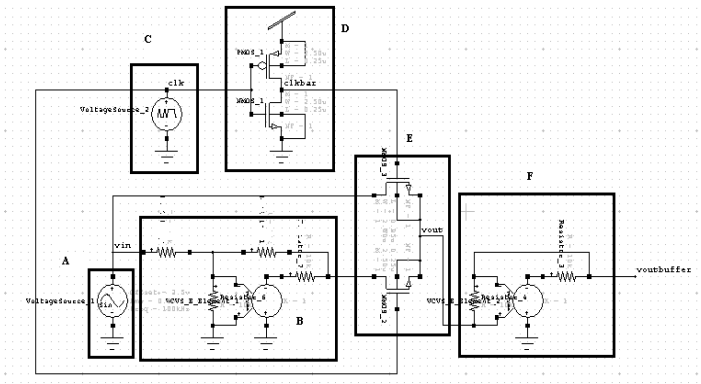

Figure 1. Schematic diagram of DSBSC Modulator

The whole circuit shown in figure 1 is divided into five blocks . Block A ,B,C,D ,E and F. Block A is consisting of message signal source . Block B is an inverting amplifier realised using voltage controlled voltage source having 2 MΩ input resistance , 75 Ω output resistance , open loop gain of 2×10^5 and two external resistances each of value 10K Ω . One 10K Ω resistance is connected between output of amplifier and inverting terminal of the amplifier . Another 10 KΩ resistance is connected between inverting terminal of the amplifier and signal source . So closed loop gain of the inverting amplifier is approximately equals to -1. Block C is for carrier signal source basically a clock pulse generator. Block D is a CMOS inverter used to invert clock pulse .Block E is the heart of the circuit .Here actual DSBSC modulation is performed using two MOS transistor only . Block F is configured for buffer amplifier with a vgoltage controlled voltage source having 2 MΩ input resistance , 75 Ω output resistance , open loop gain of 2×10^5 and shorting externally the output of voltage controlled voltage source to the inverting terminal of the same voltage controlled voltage source . Non inverting terminal of buffer is used to apply signal . So gain of the buffer is approximately equal to 1. Source terminal of Bottom MOS transistor say MNMOS_2 of block E is connected to message source in block A through block B consisting of an inverting amplifier. Message signal source in the block A is connected to source terminal of the top MOS transistor say transistor MNMOS_3 in block E of figure 1.From block C carrier signal is connected to gate terminal of bottom MOS transistor of block E of figure 1.Gate terminal of top MOS transistor in the block E is connected to carrier source through a CMOS inverter. Drain terminal of two MOS transistor in the block E is tied together to get DSBSC modulated output .Body terminal of both of transistors in block E are connected to their drain terminal to avoid body bias effect . Output from block E is connected to the non inverting terminal of buffer amplifier in the block F . Here buffer amplifier is employed to avoid loading effect . Final output is taken from buffer amplifier.

B. Circuit operation

To simulate the circuit 1Khz sine is taken as message signal . Clock pulse of frequency 50KHz is taken as carrier signal . When clock is high gate terminal of bottom MOS transistor MNMOS_2 in the block E is high .So MNMOS_2 is on and inverted message signal will be passed through MNMOS_2 to the output of block E. During high time of clock pulse as the CMOS inverter output is low. So gate terminal of top MOS transistor MNMOS_3 in the block E is low and transistor is off . On the other hand during low time of clock pulse MNMOS_2 transistor is off whereas transistor MNMOS_3 is on and message signal is passed to the output of block E through MNMOS_3.For repetition of clock pulses and observation for a message signal time period output from block E is a DSBSC modulated wave .Final output is taken from the buffer amplifier .

C. T-SPICE generated waveform

Output waveforms generated by T-SPICE software from different blocks of figure1 are displayed here . Figure 2a & 2b represents message signal and inverted message signal from block A and B block respectively. Carrier signal and inverted carrier signal are represented in figure 2c & 2d respectively .DSBSC modulated output from block E is shown in figure 2e .Output from buffer circuit is shown in figure 2f .

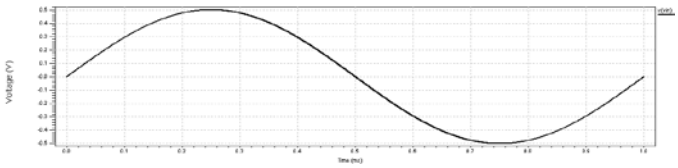

Figure 2a . Message signal

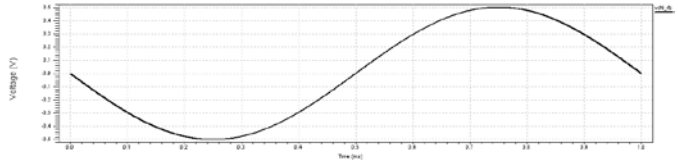

Figure 2b.Inverted message signal from out put of block B

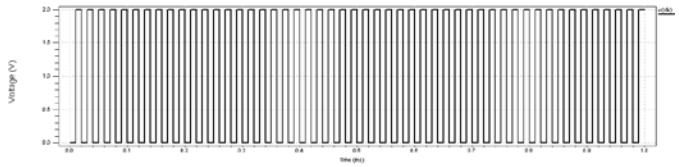

Figure 2c.Carrier signal

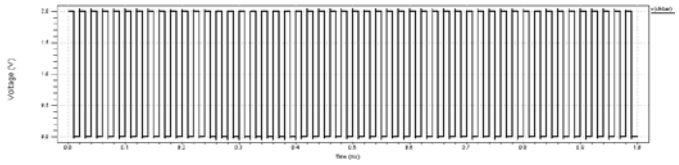

Figure 2d. Inverted carrier signal from output of block D

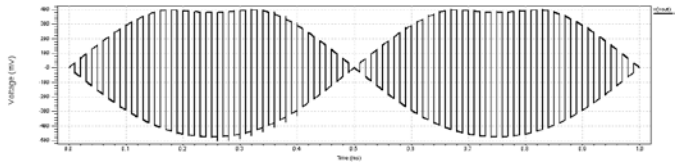

Figure 2e.DSBSC modulated waveform from output of block E

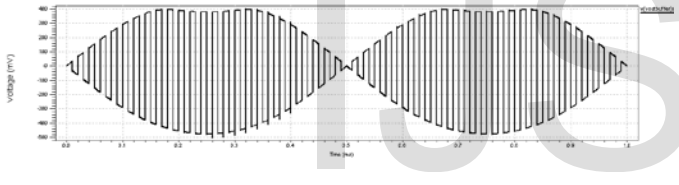

Figure 2f. DSBSC modulated waveform from buffer output termina

III. Analysis of Power

In this article power drawn from message source, power consumption in CMOS inverter and power dissipated in two 10KΩ external resistances in block B have been discussed.

A. Power drawn form message source

Ideally for any kind of circuit design no power will be drawn from signal source .But practically for all types of circuit design few power is drawn from signal source. In our case nature of instantaneous power drawn from message source is shown in figure 3a .As shown in figure 3a comparatively more power is drawn during off period of clock pulse than high period of clock. During off time of clock MNMOS_3 transistor in E block is on .As message source is directly connected to source terminal of MNMOS_3 transistor , comparatively high current is drawn from message source as drawn during on time of clock. When MNMOS_2 transistor is on during high time of clock comparatively less current is drawn from message source as inverting amplifier input resistance is high compared to the on resistance of MNMOS_3. In instantaneous power curve of figure 3a some power glitches are also observed during transition of clock pulse .As measured average power drawn from the message source is 2.36×10^{-5} Watt.

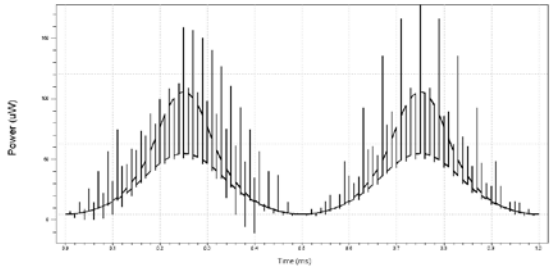

Figure 3a. Instantaneous power drawn from message source

B. Power consumption in CMOS inverter

Instantaneous power consumption in CMOS inverter is shown in figure 3b.During transition of clock both NMOS and PMOS transistor of CMOS inverter are on ,VDD is directly connected to ground and maximum power is consumed This is shown in figure 3b like a spike wave .During steady state of clock almost zero power is consumed in CMOS inverter .Average power consumed in CMOS inverter as measured is 2.02×10^{-9} Watts.

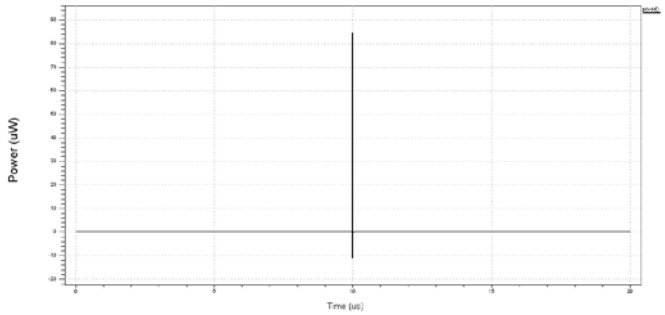

Figure 3b. Instantaneous power consumed in CMOS inverter

B. Power dissipated in two 10K Ω external resistances in block B

As the value of two resistances are same and almost same current flows through the two resistances power

dissipation across the two 10 KΩ resistances are also same . The nature of instantaneous power dissipated across one of the resistance is shown in figure 3c. Measured Power consumption across the one of the resistance is 1.25 $\times 10^{-5}$ Watt.

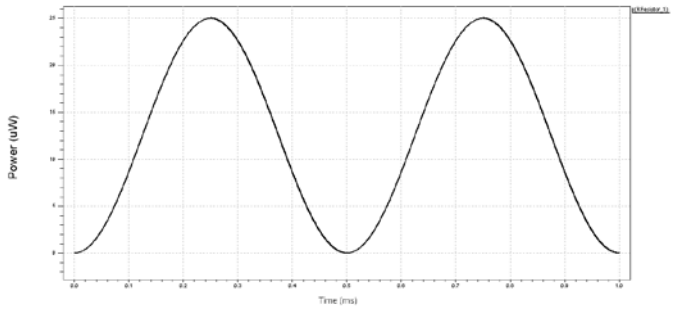

Figure 3c. Instantaneous power dissipation across 10KΩ resistance

IV. DELAY AND FREQUENCY RESPONSE

For any circuit either discrete or integrated circuit in addition with power analysis delay and frequency response analysis is also urgent to measure the performance of the circuit .

A. Delay

In our designed DSBSC modulator circuit delay between clock input (input terminal of CMOS inverter) and output terminal of buffer amplifier has been measured . Amount of delay found is 1.33×10^{-12} Sec or 1.33ps.

B. Frequency Response

Frequency response is plotted using T-SPICE as shown in figure 3d. It is seen that circuit exhibits very wide frequency response without attenuation . From frequency curve -3dB cut off frequency is approximately 188 GHz.

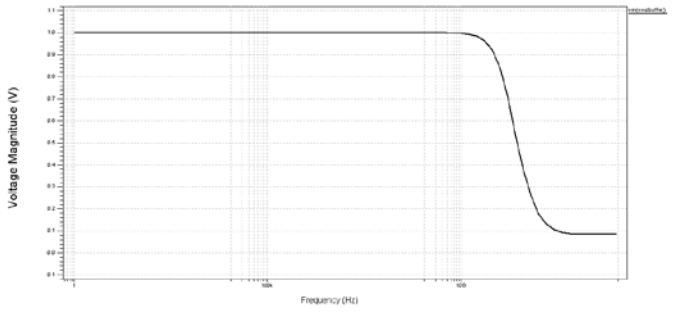

Figure 3d.Frequency response of DSBSC modulator

V. THERMAL NOISE DUE TO CHANNEL RESISTANCE OF MOS

In a circuit noise is unwanted signal .There are several types of noise exists in both integrated circuits and discrete circuits. Among all noises thermal noise and flicker are predominant in integrated circuit. In DSBSC modulator circuit of figure1 only contribution of thermal noise at buffer output due to channel resistance of MNMOS_2 is measured . It is measured the variation of said thermal noise due to temperature as shown in table 1. Figure 4 is the graphical representation of table1 .

Table1

Temperature (0C)	Thermal Noise(Square Volt/Hz)
25	1.15E-24
30	1.62E-24
35	2.27E-24
40	3.14E-24
45	4.31E-24
50	5.84E-24
55	7.85E-24
60	1.05E-23
65	1.38E-23
70	1.81E-23

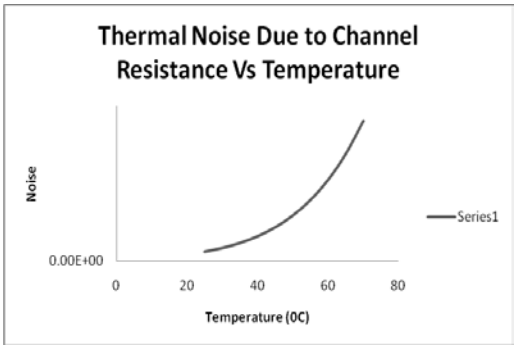

Figure 4. Variation of thermal noise at buffer output due to channel resistance of MOS transistor MNMOS_2

VI. NETLIST

Overall net list of the circuit of figure1 is presented below.

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```
RResistor_1   N_8        N_4          R=10k
RResistor_2   vin        N_8          R=10k
RResistor_3   N_5        voutbuffer   R=75
RResistor_4   voutbuffer vout         R=2MEG
RResistor_6   N_8        Gnd          R=2MEG
RResistor_7   N_9        N_4          R=75

MNMOS_1 clkbar clk Gnd Gnd nh W=0.4 5u L=.15u
AS=.3375p PS=2.4u AD=.3375p PD=2.4u

MNMOS_2 N_4 clk vout vout nh W=0.45u L=.15u
AS=.3375p PS=2.4u AD=.3375p PD=2.4u

MNMOS_3 vin clkbar vout vout nh W=0.45u L=.15u
AS=.3375p PS=2.4u AD=.3375p PD=2.4u

MPMOS_1 clkbar clk Vdd Vdd ph W=.9u L=.15u
AS=.675p PS=3.3u AD=.675p PD=3.3u

VVoltageSource_2 clk Gnd BIT({0101} pw=10u on=2
off=0 rt=.01n ft=.01n delay=0 ht=10u lt=10u )

*VVoltageSource_1 vin Gnd SIN(0 500m 1K 0 0 0)

EVCVS_E_Element_1 Gnd N_9 Gnd N_8 2E+5
EVCVS_E_Element_2 Gnd N_5 vout voutbuffer 2E+5

v12 vin gnd AC 1V

 vdd vdd gnd 2
.include "E:\\dual.md"

 .temp 70
*.tran .1n 20u

*.power VVoltageSource_1 .1n 40u

.ac dec 5 1HZ 100KHZ

.noise voutbuffer gnd

*.measure tran delay trig v(clk) val=1 rise=2 targ
v(voutbuffer) val=0 fall=2

.print noise dn(MNMOS_2,ID)

*.ac dec 5 0 .000001HZ 1000000000000HZ

*.print clk voutbuffer

*.print ac vm(voutbuffer)

*.print p(VVoltageSource_1)
.end
```

CONCLUSION

The DSBSC modulator circuit is designed with MOS transistor having channel length of 150nm. Power drawn from the message source is about 23 micro watt. Power consumption in CMOS inverter section is of the order of nano watt .Power consumed in each of 10KΩ resistance in inverting amplifier block is 1.25×10^{-5} Watt. Delay measured from clock input to buffer amplifier output is 1.33ps.Higher cut off frequency from frequency response plot is around 188GHz. Thermal noise found at the buffer output terminal is due to channel resistance of one of the MOS transistor in the modulator section is of the order of 10^{-24} $Volt^2$ /Hz. Although the amount of noise is very less and tense to zero sometimes this amount of noise is also considered along with other types of noises for design purpose .The circuit of figure1 can be fabricated in two way : considering D and E block only and connecting B and F block externally or considering all B,C,D,E,F blocks . If one would like to fabricate the circuit considering later option it is necessary to replace the equivalent of voltage controlled voltage source in both B and F block by circuit using Mos transistor . It is also necessary to use lower resistance irrespective of using 10 KΩ resistances because fabrication of very high value resistance takes very large space and circuit becomes bulkier.

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